

In re Patent Application of:

BREWER

Serial No. **09/674,444**

Filed: **OCTOBER 31, 2000**

REMARKS

Claims 1 to 3, 5 to 12 and 15 to 23 are pending.

The claims have been amended to more particularly define the invention in a manner which is believed to patentably distinguish the invention over the cited prior art. Reconsideration of this application in light of the foregoing amendments and following remarks is respectfully requested.

More specifically, independent claims 1, 10 and 15 have been amended to more concisely define the reference clock signal as a "jitter-free" clock signal formed from the original digital signal, as disclosed on Page 8, line 11 of the application. These claims have also been amended to more clearly specify that the digital signal is sampled by the reference clock signal, whereby a jitter measurement can be determined based on occasions when the number of sampling times in any bit of said digital signal is different from a predetermined number.

As a result of these amendments, it is respectfully submitted that these claims, and the claims dependent thereon, define subject matter that is neither disclosed nor suggested by the prior art relied upon in the outstanding Office Action. As such, each ground of rejection under 35 U.S.C. 102 and 35 U.S.C. 103 is respectfully traversed, and applicant respectfully requests favorable reconsideration of all the claims.

More particularly, the system disclosed in the Hamre reference uses two clock signals, i.e. a nominal clock and an

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early clock, both of which are derived from the data signal and can be expected to contain jitter, which may not matter, since the results of the early clock are compared to those of the nominal clock. As a result, only a positive jitter peak can be established based on a statistical error rate performance of the early clock relative to the nominal clock.

Applicant's claimed invention eliminates the need for both nominal and early clock signals by counting the number of pulses from a single "offset", "jitter-free" reference clock signal that fall in each bit of the digital signal, and comparing that count to a predetermined number that would occur if there was no jitter. Then, the number of times that the number of sampling times in any bit of the digital signal is different from the predetermined number is counted and, from this count, jitter is determined.

The clock signal according to the present invention is "offset" from the data signal, not just another clock signal, i.e. the delayed clock signal, as in the Hamre reference. In accordance with the claimed invention, the combination of offsetting and making the reference clock signal jitter free enables a single clock signal to indicate those occasions when the number of sampling times in any bit of the digital signal is different from the predetermined number, so that the number of occasions derived from the single reference clock signal may be used to provide both low and high frequency jitter measurements.

Applicant's claimed invention is much simpler than the device disclosed in the Hamre reference, i.e., it does not require the hardware to generate both the nominal and early

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clock signals, and enables the recovery of both a positive and negative peak by looking for any errors, not just statistical error rate information.

The secondary reference to Toshimura has been cited to show circuitry for "clock-smoothing". However, like Hamre, Toshimura does not disclose or suggest the above-referenced features, including counting the number of pulses from a single offset, jitter-free reference clock in each clock signal bit, and comparing that count to a number that would occur without jitter.

As a consequence, it is respectfully submitted that the foregoing amendments place all of the claims remaining in the application in condition for allowance. Early and favorable consideration is, accordingly, earnestly solicited.

Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Please charge any shortage in fees due in connection with the filing of this paper, including Extension of Time fees, to Deposit Account No. 50-1465 and please credit any excess fees to such deposit account.

Respectfully submitted,



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